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APPLICATION FOR LETTERS PATENT

Title : DISPLAY DEVICE AND DRIVING METHOD OF THE SAME

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority of Japanese Patent Applications No. 2000-211661, filed on July 12, 2000, the contents being incorporated herein by reference.

BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to display devices and driving methods of the devices, particularly to display devices that make a display in accordance with a scanning signal supplied from a scanning driver, and driving methods of the devices.

[Description of the Related Art]

In recent research and development of liquid crystal display devices, keen competition is held for technologies for cost reduction. In particular, a technique of forming a polysilicon thin-film transistor by a low-temperature process makes it possible to form not only a display area but also a peripheral circuit (e.g., a driver) on an inexpensive glass substrate. This technique has received a great deal of attention because the conventional cost of mounting driver ICs (Integrated Circuits) is reduced, and large cost reduction can be expected. Attempts have been made to form a polysilicon thin-film transistor on a glass substrate to manufacture a large and highly precise liquid crystal display

device.

Fig. 22 shows the structure of a liquid crystal display device according to the first prior art. A display area 100 has two-dimensionally arrayed thin-film transistors. Each thin-film transistor controls display on the corresponding pixel. A first scanning driver 101a is arranged on the left side of the display area 100, while a second scanning driver 101b is arranged on the right side of the display area 100. The first and second scanning drivers 101a and 101b supply identical scanning signals to two ends of each scanning line of the display area 100 through n output lines GL1 to GLn and n output lines GR1 to GRn, respectively. First and second data drivers 102a and 102b are arranged on the upper and lower sides of the display area 100 to supply data signals to the display area 100.

A disconnection point 103 disconnects, in the display area 100, a scanning line for connecting the output line GL3 of the first scanning driver 101a and the output line GR3 of the second scanning driver 101b. In this case, since a scanning signal is supplied from the first scanning driver 101a to a display area 103a, display in the display area 103a is enabled. On the other hand, a scanning signal is supplied from the second scanning driver 101b to a display area 103b, so display in the display area 103b is enabled. That is, even when disconnection

occurs at the disconnection point 103, display is enabled in both the display areas 103a and 103b. For this purpose, the two, first and second scanning drivers 101a and 101b are prepared.

Along with the recent increase in resolution of liquid crystal display devices, the numbers of output lines GL1 to GLn and GR1 to GRn of the scanning drivers 101a and 101b are increasing. As a consequence, defects on the manufacturing process readily occur in the scanning drivers 101a and 101b at high probability.

For example, the output line GR3 may be short-circuited to a power supply line or a ground line at a short-circuit point 104 in the scanning driver 101b due to a defect on the manufacturing process, as shown in Fig. 23. In this case, the output line GR3 in the scanning driver 101b is fixed to the power supply potential or ground potential, so no normal scanning signal is supplied from the scanning driver 101b to the display area 100. As a result, the right region of a horizontal line in the display area 100, which corresponds to the output line GR3, always displays white or black, and normal display is impeded.

As described above, even when the display area 100 has no defect, a defect in the scanning driver 101a or 101b makes the liquid crystal display device defective because the display area and scanning

drivers are formed on a single glass substrate. A technique of correcting a defect in the scanning driver 101a or 101b has been proposed. This technique will be described next.

Fig. 24 shows the structure of a liquid crystal display device according to the second prior art disclosed in Japanese Patent Application Laid-open No. 6-67200. The liquid crystal display device of the second prior art is constructed by adding n-channel MOS (Metal Oxide Semiconductor) transistors 111a and 111b to the liquid crystal display device of the first prior art (Figs. 22 and 23). A control signal is supplied to the gates of the transistors 111a through a control signal terminal CL. The sources and drains of the transistors 111a are connected to output lines GL1 to GLn of a first scanning driver 101a and the scanning lines in a display area 100, respectively. Similarly, a control signal is supplied to the gates of the transistors 111b through a control signal terminal CR. The sources and drains of the transistors 111b are connected to output lines GR1 to GRn of a second scanning driver 101b and the scanning lines in the display area 100, respectively.

Assume that it is detected after manufacturing the liquid crystal display device that the output line GR2 short-circuits to the power supply line or ground line at a short-circuit point 112 in the

second scanning driver 101b. In this case, a high-level voltage is applied to the control signal terminal CL, and a low-level voltage is applied to the control signal terminal CR.

Consequently, the high-level voltage is applied to the gates of all of the n transistors 111a, and the n transistors 111a are turned on to connect the output lines GL1 to GLn of the scanning driver 101a to the scanning lines in the display area 100. A scanning signal is supplied from the scanning driver 101a to the display area 100.

On the other hand, the low-level voltage is applied to the gates of all of the n transistors 111b, and the n transistors 111b are turned off to disconnect the output lines GR1 to GRn of the scanning driver 101b from the scanning lines in the display area 100. No scanning signal is supplied from the scanning driver 101b to the display area 100.

That is, since a normal scanning signal is supplied only from the scanning driver 101a to the display area 100, normal display is possible. However, Japanese Patent Application Laid-open No. 6-67200 discloses no method of detecting the short-circuit point 112. Additionally, even if the defect in the second line can be visually detected on the display screen, it cannot be determined whether the defect in the second line is due to a short circuit in the scanning driver 101a or in the

scanning driver 101b. Without presenting the determination method, which scanning driver has a defect, the first scanning driver 101a or second scanning driver 101b, cannot be known, and the voltage levels for the control signal terminals CL and CR cannot be determined.

Furthermore, as shown n Fig. 25, the output line GR2 may short-circuit at a short-circuit point 113 in the second scanning driver 101b, and simultaneously, a scanning line may be disconnected at a disconnection point 114 in the display area 100. In this case, assume that a high-level voltage is applied to the control signal terminal CL, and a low-level voltage is applied to the control signal terminal CR to correct the short-circuit point 113, as described above.

As a result, although a scanning signal is supplied from the first scanning driver 101a to a display area 114a, no scanning signal is supplied from either of the scanning driver 101a and 101b to a display area 114b, so normal display is disabled in the display area 114b.

Also, as shown in Fig. 26, assume a case wherein the output line GL4 short-circuits at a short-circuit point 115 in the first scanning driver 101a, the output line GR1 short-circuits at a short-circuit point 116 in the second scanning driver 101b, and a scanning line is disconnected at a disconnection

point 117 in the display area 100.

To correct the short-circuit point 116, a low-level voltage is applied to the control signal terminal CR, and a high-level voltage is applied to the control signal terminal CL. In this case, however, since the transistors 111b are turned off, and no scanning signal is supplied to a display area 117b, normal display is disabled in the display area 117b. In addition, since the output line GL4 short-circuits at the short-circuit point 115 in the first scanning driver 101a, no normal scanning signal is supplied to the fourth scanning line in the display area 100 from either of the second scanning driver 101b and the first scanning driver 101a. For this reason, the fourth line cannot be normally displayed.

On the other hand, to correct the short-circuit point 115, a low-level voltage is applied to the control signal terminal CL, and a high-level voltage is applied to the control signal terminal CR. In this case, however, since the transistors 111a are turned off, and no scanning signal is supplied to a display area 117a, normal display is disabled in the display area 117a. In addition, since the output line GR1 short-circuits at the short-circuit point 116 in the second scanning driver 101b, no normal scanning signal is supplied to the first line in the display area 100 either from the first scanning

driver 101a nor from the second scanning driver 101b. For this reason, the first line cannot be normally displayed.

The above defects cannot be completely corrected. Additionally, Japanese Patent Application Laid-open No. 6-67200 presents no defect detection method, as described above. A publication that presents a defect detection method will be described next.

Fig. 27 shows the structure of a liquid crystal display device according to the third prior art disclosed in Japanese Patent No. 2973969. The liquid crystal display device of the third prior art is constructed by adding n-channel MOS transistors 121a and 121b to the liquid crystal display device of the first prior art (Figs. 22 and 23).

Output lines GL1 to GLn of a first scanning driver 101a are connected to the gates of the n transistors 121a. An input terminal Lin and output terminal Lout are connected to the sources and drains of the n transistors 121a.

On the other hand, output lines GR1 to GRn of a second scanning driver 101b are connected to the gates of the n transistors 121b. An input terminal Rin and output terminal Rout are connected to the sources and drains of the n transistors 121b.

When a check signal is input to the input terminal Lin, and the signal from the output terminal Lout is checked, the state of a scanning signal

supplied to the gates of the transistors 121a can be known. In addition, when a check signal is input to the input terminal Rin, and the signal from the output terminal Rout is checked, the state of a scanning signal supplied to the gates of the transistors 121b can be known. However, the third prior art discloses only the check method and no correction method.

As described above, the second prior art presents a correction method but no check method. The correction method has limitations and cannot correct the defects shown in Figs. 25 and 26.

The third prior art discloses a check method but no correction method. Details of the check method are not presented, and all defects cannot always be detected. Even if a defect can be detected, how to correct the defect is not described.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a display device capable of detecting a defect with which the potential of an output line of a scanning driver is fixed or unfixed and automatically correcting the defect, and a driving method of the device.

It is another object of the present invention to provide a display device capable of reliably detecting a defect with which the potential of an

output line of a scanning driver is fixed or unfixed, and a driving method of the device.

It is still another object of the present invention to provide a display device capable of reliably correcting a defect with which the potential of an output line of a scanning driver is fixed or unfixed, and a driving method of the device.

A display device according to the present invention comprises a display section with scanning lines, and a scanning driver with output lines for supplying scanning signals to the scanning lines in the display section. When the potential of at least one of the output lines of the scanning driver is fixed or unfixed due to an error in the scanning driver or the like, the output line with the fixed or unfixed potential is disconnected from the corresponding scanning line in the display section.

When the potential of an output line of the scanning driver is fixed or unfixed, only the output line with the fixed or unfixed potential can be disconnected from the corresponding scanning line in the display section. For example, when an output line of the first scanning driver is disconnected from the corresponding scanning line in the display section, a normal scanning signal is supplied from the corresponding output line of the second scanning driver to the scanning line in the display section. Instead of disconnecting all the output lines of the

first or second scanning driver from all the scanning lines in the display section, only the output line with the fixed potential can be disconnected from the scanning line in the display section. For this reason, the normal output lines of the first or second scanning driver and the scanning lines in the display section are connected, so normal display can be performed. In addition, since it is determined individually for the first and second scanning drivers whether the potential of an output line is fixed or unfixed, and the output lines are individually disconnected from the scanning lines as needed, even defects as shown in Figs. 25 and 26 can be corrected. That is, even when defects are present at portions, e.g., both of the first or second scanning driver and the display section have defects, or the first and second scanning drivers and display section have defects, the defects can be reliably detected and automatically corrected, so normal display can be performed.

Even when the scanning driver has a defect or the scanning driver and display section have defects, the defect can be automatically corrected, so normal display can be performed. In addition, since the automatic correction of the display device is possible, the yield of display devices can be increased, the productivity can be improved, and the cost of display devices can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of a liquid crystal display device according to the first embodiment of the present invention;

Fig. 2 is a circuit diagram showing the structure of a display area;

Fig. 3 is a circuit diagram showing the structure of a data driver;

Fig. 4A is a view showing a clocked inverter;

Fig. 4B is a circuit diagram showing the structure of the clocked inverter;

Fig. 5A is a circuit diagram showing the structure of a scanning driver;

Fig. 5B is a timing chart showing the operation of the scanning driver;

Fig. 6 is a circuit diagram of a judging unit according to the first embodiment and its peripheral portion;

Fig. 7 is a timing chart showing the operation of the liquid crystal display device according to the first embodiment;

Fig. 8 is a block diagram showing the structure of a liquid crystal display device according to the second embodiment of the present invention;

Fig. 9 is a block diagram showing the structure of a liquid crystal display device according to the third embodiment of the present invention;

Fig. 10 is a circuit diagram of a judging unit according to the third embodiment and its peripheral portion;

Fig. 11 is a timing chart showing operation when the liquid crystal display device according to the third embodiment is normal;

Fig. 12 is a timing chart showing operation when a scanning line in a scanning driver of the liquid crystal display device according to the third embodiment is fixed at high level;

Fig. 13 is a circuit diagram of a judging unit and its peripheral portion in a liquid crystal display device according to the fourth embodiment of the present invention;

Fig. 14 is a timing chart showing operation when the liquid crystal display device according to the fourth embodiment is normal;

Fig. 15 is a timing chart showing operation when a scanning line in a scanning driver of the liquid crystal display device according to the fourth embodiment is fixed at high level;

Fig. 16 is a timing chart showing operation when two scanning lines adjacent to each other in the scanning driver of the liquid crystal display device according to the fourth embodiment are fixed at high level;

Fig. 17 is a block diagram showing the structure of a liquid crystal display device according to the

fifth embodiment of the present invention;

Fig. 18 is a circuit diagram of a judging unit according to the fifth embodiment of the present invention and its peripheral portion;

Fig. 19 is a timing chart showing operation when the liquid crystal display device according to the fifth embodiment is normal;

Fig. 20 is a timing chart showing operation when a scanning line in a scanning driver of the liquid crystal display device according to the fifth embodiment is fixed at low level;

Fig. 21 is a timing chart showing operation when a scanning line in a scanning driver of the liquid crystal display device according to the fifth embodiment is fixed at high level;

Fig. 22 is a block diagram showing a case wherein the display area of a liquid crystal display device according to the first prior art has a defect;

Fig. 23 is a block diagram showing a case wherein a scanning driver of the liquid crystal display device according to the first prior art has a defect;

Fig. 24 is a block diagram showing a case wherein a scanning driver of a liquid crystal display device according to the second prior art has a defect;

Fig. 25 is a block diagram showing a case wherein the display area and scanning driver of the liquid crystal display device according to the second prior art have defects;

Fig. 26 is a block diagram showing a case wherein the display area and first and second scanning drivers of the liquid crystal display device according to the second prior art have defects; and

Fig. 27 is a block diagram showing the structure of a liquid crystal display device according to the third prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described below with reference to drawings.

(First Embodiment)

Fig. 1 is a block diagram showing the structure of a liquid crystal display device according to the first embodiment of the present invention. When an output line in a first or second scanning driver 4a or 4b has a short circuit to the ground line or disconnection and is fixed at low level or unfixed, the liquid crystal display device according to the first embodiment can detect the defect and automatically correct it.

In addition to a display area 2, a first scanning driver 4a, a second scanning driver 4b, a first data driver 3a, and a second data driver 3b, judging units 5a and 5b and n-channel MOS transistors 7a, 7b, 8a, and 8b are integrally formed on a glass substrate 1. The space between the glass substrate 1 and a counter substrate 6 is filled with liquid crystal. Counter

electrodes are formed on the entire surface of the counter substrate 6. The second to fifth embodiments to be described later also use similar counter substrates 6. All transistors to be described in this specification are polysilicon thin-film transistors.

Fig. 2 shows a specific structure of a region 9 in the display area (display section) 2. The display area 2 has n-channel MOS transistors 21 arrayed in a two-dimensional matrix. A left-end portion L1 of a scanning line and a right-end portion R1 of the scanning line are connected to each other to form a first scanning line. A left-end portion L2 of another scanning line and a right-end portion R2 of this scanning line are connected to each other to form a second scanning line. In a similar way, a left-end portion Ln of a scanning line and a right-end portion Rn of this scanning line are connected to each other to form an nth scanning line. The gates of the transistors 21 are connected to the scanning lines (L1,R1) to (Ln,Rn) extending in the horizontal direction, and the sources and drains are connected to data lines D1 to Dn extending in the vertical direction and pixel electrodes 22, respectively. When a predetermined potential is applied to each pixel electrode 22, display on the corresponding pixel can be controlled.

Referring to Fig. 1, the first and second

scanning drivers 4a and 4b are arranged on both sides of the display area 2 to sandwich the display area 2 and have output lines GL1 to GLn and GR1 to GRn to supply identical scanning signals to the ends of the scanning lines L1 to Ln and R1 to Rn in the display area 2.

The first scanning driver 4a is arranged on the left side of the display area 2 and has the n output lines GL1 to GLn. The output lines GL1 to GLn of the first scanning driver 4a are connected to the scanning lines L1 to Ln in the display area 2 through the n n-channel MOS transistors (switching units) 8a, respectively. That is, the sources and drains of the n transistors 8a are connected to the output lines GL1 to GLn and scanning lines L1 to Ln, respectively.

The second scanning driver 4b is arranged on the right side of the display area 2 and has the n output lines GR1 to GRn. The output lines GR1 to GRn of the second scanning driver 4b are connected to the scanning lines R1 to Rn in the display area 2 through the n n-channel MOS transistors (switching units) 8b, respectively. That is, the sources and drains of the n transistors 8b are connected to the output lines GR1 to GRn and scanning lines R1 to Rn, respectively.

The first and second data drivers 3a and 3b are arranged on two sides of the display area 2 to sandwich the display area 2. The first data driver 3a is arranged on the upper side of the display area

2 to supply data signals to the odd-numbered lines D1, D3, D5,..., Dn-1 in the display area 2. The second data driver 3b is arranged on the lower side of the display area 2 to supply data signals to the even-numbered lines D2, D4, D6,..., Dn in the display area 2. The first and second data drivers 3a and 3b need not be separated and may be integrated to one data driver. However, when the first and second data drivers 3a and 3b are separated, the wiring pitch of them can be made large. This relaxes the manufacturing process conditions and facilitates manufacturing.

The relationship between the scanning drivers 4a and 4b and the data drivers 3a and 3b will be described next. The first scanning driver 4a outputs a scanning signal for sequentially selecting the scanning lines (L1,R1) to (Ln,Rn) in the display area 2 to the output lines GL1 to GLn. The second scanning driver 4b similarly outputs a scanning signal for sequentially selecting the scanning lines (L1,R1) to (Ln,Rn) in the display area 2 to the output lines GR1 to GRn.

When the first scanning line (L1,R1) is selected, the data drivers 3a and 3b output data D1 to Dn corresponding to the first scanning line (L1,R1). When the second scanning line (L2,R2) is selected, the data drivers 3a and 3b output data D1 to Dn corresponding to the second scanning line (L2,R2).

Subsequently, the data drivers 3a and 3b sequentially output data up to the n-th scanning line (Ln,Rn).

The gates of the n first check transistors (n-channel MOS transistors) 7a are connected to the output lines GL1 to GLn of the first scanning driver 4a, respectively. One of the source and drain of each of the n first check transistors 7a is connected to a check input terminal Lin, and the other is connected to the input terminal of the judging unit 5a.

A check signal is input to the input terminal Lin. When one of the output lines GL1 to GLn is selected, the transistor 7a connected to the selected output line is turned on. The transistor 7a then outputs (transmits) the check signal input from the input terminal Lin to the judging unit 5a. If the first scanning driver 4a is normal, the n transistors 7a are sequentially turned on from the transistor corresponding to the first output line GL1 to that corresponding to the n-th output line GLn.

A case wherein the first scanning driver 4a is normal will be described first. Each transistor 7a is turned on every time the scanning signal on the corresponding one of the output lines GL1 to GLn goes high (every time the output line is selected). Then, the judging unit 5a normally receives the check signal, determines that the scanning signal on the output lines GL1 to GLn of the first scanning driver

4a is normal, and outputs a high-level signal. This determination is done at the timing of each of the output lines GL1 to GLn.

The gates of the n switching transistors (n-channel MOS transistors) 8a are connected to the output terminal of the judging unit 5a. One of the source and drain of each of the n switching transistors 8a is connected to the corresponding one of the output lines GL1 to GLn of the scanning driver 4a, and the other is connected to the corresponding one of the scanning lines L1 to Ln in the display area 2.

When the judging unit 5a outputs a high-level signal, the n-channel transistors 8a are turned on to connect the output lines GL1 to GLn of the scanning driver 4a to the scanning lines L1 to Ln in the display area 2, respectively. Thus, the display area 2 can receive the scanning signal from the first scanning driver 4a and perform normal display.

A defect with which one or more output lines in the first scanning driver 4a short-circuit to the ground line, and the scanning signals on the output lines are fixed at low level, or a defect with which one or more output lines are disconnected and unfixed will be considered next. When a scanning signal is fixed at low level or unfixed, the transistor 7a corresponding to the scanning signal is kept off. The judging unit 5a cannot obtain the check signal

input from the terminal Lin, and therefore determines that a predetermined one of the output lines GL1 to GLn of the first scanning driver 4a short-circuits to the ground line or is unfixed, and outputs a low-level signal. The judging unit 5a does this determination for each of the output lines GL1 to GLn and outputs a signal. That is, the judging unit 5a outputs a high-level signal at the timing of a normal output line and a low-level signal at the timing of an abnormal output line.

When the judging unit 5a outputs a low-level signal, the n-channel MOS transistors 8a are turned off to disconnect the output lines GL1 to GLn of the scanning driver 4a from the scanning lines L1 to Ln in the display area 2. For a normal output line, the judging unit 5a outputs a high-level signal, so the transistors 8a are turned on to connect the output lines GL1 to GLn to the scanning lines L1 to Ln. Thus, the display area 2 receives the scanning signal only from a normal output line of the first scanning driver 4a. For an abnormal output line, the display area 2 can receive the scanning signal from the second scanning driver 4b and perform normal display.

The first scanning driver 4a, the transistors 7a and 8a, and the first judging unit 5a have been described above. This also applies to the second scanning driver 4b, the transistors 7b and 8b, and the second judging unit 5b.

More specifically, the gates of the transistors 7b are connected to the output lines GR1 to GRn of the second scanning driver 4b. One of the source and drain of each of the transistors 7b is connected to a check input terminal Rin, and the other is connected to the input terminal of the judging unit 5b.

The gates of the transistors 8b are connected to the output of the judging unit 5b. One of the source and drain of each of the transistors 8b is connected to the corresponding one of the output lines GR1 to GRn of the second scanning driver 4b, and the other is connected to the corresponding one of the scanning lines R1 to Rn in the display area 2.

The transistors 7b switch in accordance with the scanning signals on the output lines GR1 to GRn of the second scanning driver 4b. The judging unit 5b determines in accordance with the switching states of the transistors 7b whether the output lines GR1 to GRn of the second scanning driver 4b are short-circuited to the ground line or unfixed and outputs the determination result. The transistors 8b switch connection between the output lines GR1 to GRn of the second scanning driver 4b and the scanning lines R1 to Rn in the display area 2 in accordance with the output from the judging unit 5b.

A case wherein the liquid crystal display device has three defects will be described next. As the first defect, the output line GLn in the first

scanning driver 4a short-circuits to the ground line at a short-circuit point 10. As the second defect, the output line GR2 in the second scanning driver 4b short-circuits to the ground line at a short-circuit point 11. As the third defect, the scanning line (L5,R5) in the display area 2 is disconnected at a disconnection point 12.

In this case, the judging unit 5a determines that only the output line GLn of the first scanning driver 4a short-circuits to the ground line, and the remaining output lines GL1 to GLn-1 are normal. Only the transistor 8a corresponding to the n-th output line GLn is turned off, and the remaining transistors 8a corresponding to the output lines GL1 to GLn-1 are turned on.

The judging unit 5b determines that only the output line GR2 of the second scanning driver 4b short-circuits to the ground line, and the remaining output lines GR1 and GR3 to GRn are normal. Only the transistor 8b corresponding to the second output line GR2 is turned off, and the remaining transistors 8b corresponding to the output lines GR1 and GR3 to GRn are turned on.

As a consequence, the second scanning line (L2,R2) in the display area 2 receives the scanning signal only from the first scanning driver 4a, and the n-th scanning line (Ln.Rn) receives the scanning signal only from the second scanning driver 4b. The

remaining scanning lines (L1,R1) and (L3,R3) to (Ln-1,Rn-1) receive the scanning signals from both of the first and second scanning drivers 4a and 4b.

Near the disconnection point 12, a display area 12a can perform normal display upon receiving the scanning signal from the first scanning driver 4a. On the other hand, a display area 12b can perform normal display upon receiving the scanning signal from the second scanning driver 4b. In this way, even when defects are present at the three points 10 to 12, all lines can be normally displayed.

Fig. 3 is a circuit diagram showing the structure of the data driver 3a shown in Fig. 1. The structure of the first data driver 3a will be described, though the second data driver 3b has the same structure as that of the first data driver 3a. The first data driver 3a has a shift register 31, a video analog line 32, and an analog switch 33.

The shift register 31 receives signals from three input terminals, i.e., a start signal terminal SI, a clock terminal CLK, and a clock bar (inversion) terminal /CLK, and sequentially outputs pulses from output lines 37, 38,.... First, the output line 37 is selected, and the output line 38 is selected next, so that the subsequent output lines are sequentially selected. There are not only the two output lines 37 and 38 but actually a number of output lines. The symbol "/" means a bar (inversion) signal.

The video analog line 32 comprises, e.g., eight video analog lines 32a to 32h and supplies, e.g., the analog voltages of data signals of 256 gray levels. In the analog switch 33, an n-channel MOS transistor 34 and a p-channel MOS transistor 35 constitute a switch, and eight switches arrayed in the horizontal direction construct one unit. More specifically, in the eight units at the left end, the output line 37 is connected to the gates of the n-channel MOS transistors 34, and also connected to the gates of the p-channel MOS transistors 35 through a logic inversion circuit (inverter) 36. In the next eight units on the right side, the output line 38 is connected to the gates of the n-channel MOS transistors 34, and also connected to the gates of the p-channel MOS transistors 35 through another logic inversion circuit (inverter) 36.

The sources and drains of the n-channel MOS transistors 34 and the p-channel MOS transistors 35 are connected to the video analog lines 32a to 32h and the data lines D1, D3,..., Dn-1 in the display area 2.

When the output line 37 is selected and goes high, the eight switch units at the left end in the analog switch 33 are turned on to connect the eight video analog lines 32a to 32h to the eight data lines D1, D3,..., D15, respectively, so eight data signals are supplied to the display area 2.

After the output line 37 goes low, new data signals are supplied to the video analog line 32, and the output line 38 is selected and goes high. The eight second switch units from the left end in the analog switch 33 are then turned on to connect the eight video analog lines 32a to 32h to the eight data lines D17, D19,..., D31, respectively, so new eight data signals are supplied to the display area 2. In the above way, data are sequentially supplied up to the data line Dn-1, and data supply for one line is ended. This operation is executed for each line in the display area 2.

Fig. 4A is a diagram showing a clocked inverter used in each of the scanning drivers 4a and 4b shown in Fig. 1. The clocked inverter inverts a signal input from an input terminal IN using the clock signal CLK and clock bar signal /CLK as control signals, and outputs the inverted signal from an output terminal OUT.

Fig. 4B is a circuit diagram showing the structure of the clocked inverter shown in Fig. 4A. A p-channel MOS transistor 41 has its gate connected to the clock bar signal terminal /CLK, its source connected to a positive potential Vdd, and its drain connected to the source of a p-channel MOS transistor 42. The p-channel MOS transistor 42 has its gate connected to the input terminal IN and its drain connected to the output terminal OUT. An n-channel

MOS transistor 43 has its gate connected to the input terminal IN, its drain connected to the output terminal OUT, and its source connected to the drain of an n-channel MOS transistor 44. The n-channel MOS transistor 44 has its gate connected to the clock signal terminal CLK and its source connected to a ground potential GND.

Fig. 5A is a circuit diagram showing the structure of the first scanning driver 4a shown in Fig. 1. The structure of the first scanning driver 4a will be described below, though the structure of the second scanning driver 4b is the same as that of the first scanning driver 4a. In first clocked inverters 51 and 56, the positions of the clock signal terminal CLK and clock bar signal terminal /CLK are the same as in Fig. 4B. On the other hand, in second clocked inverters 53 and 54, the positions of the clock signal terminal CLK and clock bar signal terminal /CLK are opposite to those shown in Fig. 4B: the clock signal terminal CLK is connected to the gate of the transistor 41, and the clock bar signal terminal /CLK is connected to the gate of the transistor 44.

The clocked inverter 51 has its input connected to the start signal terminal SI and its output connected to the input of an inverter 52. The clocked inverter 53 has its input connected to the output of the inverter 52 and its output connected to

the input to the inverter 52. The clocked inverter 54 has its input connected to the output of the inverter 52 and its output connected to the input of an inverter 55. The clocked inverter 56 has its input connected to the output of the inverter 55 and its output connected to the input of the inverter 55. The clocked inverters 51 and 53 and the inverter 52 construct an odd-numbered unit, and the clocked inverters 54 and 56 and the inverter 55 construct an even-numbered unit. The odd-numbered unit and even-numbered unit are alternately repeatedly connected in the horizontal direction on the right side of the drawing.

An AND circuit 57 performs an AND operation between the output from the inverter 52 and that from the inverter 55 and outputs the result to the first output line GL1. An AND circuit 58 performs an AND operation between the output from the inverter 55 and that from the next inverter and outputs the result to the second output line GL2.

Fig. 5B is a timing chart for explaining the operation of the scanning driver 4a shown in Fig. 5A. The scanning driver 4a functions like a shift register. More specifically, when a start signal pulse is input to the start signal terminal SI, the scanning driver 4a sequentially outputs pulses to the first output line GL1, the second output line GL2,..., the n-th output line GLn.

Fig. 6 is a circuit diagram of the judging unit 5a shown in Fig. 1 and its peripheral portion. The scanning driver 4a has the same structure as that of the scanning driver 4a shown in Fig. 5A. The n-channel MOS transistors 7a correspond to the transistors 7a shown in Fig. 1. The n-channel MOS transistors 8a correspond to the transistors 8a shown in Fig. 1. The judging unit 5a corresponds to the judging unit 5a shown in Fig. 1, which is constructed by connecting two inverters 61 and 62 in series and has a function of shaping a signal received from a line Lout to H/L. The judging unit 5b and its peripheral portion have the same arrangement as that of the judging unit 5a and its peripheral portion.

Fig. 7 is a timing chart showing the operation of the liquid crystal display device (Fig. 1) according to the first embodiment. A case wherein the defects are present at the short-circuit points 10 and 11 and disconnection point 12, as shown in Fig. 1, will be exemplified.

Pulsed check signals are supplied to the check input terminals Lin and Rin. Normal pulses are sequentially output to the output lines GL1 to GLn-1. That is, a pulse is generated in the first output line GL1 at a timing T1, a pulse is generated to the second output line GL2 at a timing T2, and a pulse is generated to the third output line GL3 at a timing T3.

The n-th output line GLn is fixed at low level

because it short-circuits to the ground line at the short-circuit point 10, and no pulse is output at a timing Tn when a pulse should be output.

Similarly, normal pulses are sequentially output to the output lines GR1 and GR3 to GRn. That is, a pulse is generated in the first output line GR1 at the timing T1, a pulse is generated in the third output line GR3 at the timing T3, and a pulse is generated in the n-th output line GRn at the timing Tn.

The second output line GR2 is fixed at low level because it short-circuits to the ground line at the short-circuit point 11, and no pulse is output at the timing T2 when a pulse should be output.

The signal from the check input terminal Lin is transmitted to the output line Lout (Fig. 6) to the judging unit 5a through the transistors 7a. Since the output lines GL1 to GLn-1 are normal, the signal from the check input terminal Lin directly appears on the output line Lout at the timings T1 to Tn-1. However, since the output line GLn is fixed at low level, the transistor 7a is turned off to change the output line Lout to low level at the timing Tn.

In a similar manner, the signal from the check input terminal Rin is transmitted to an output line Rout to the judging unit 5b through the transistors 7b. Since the output lines GR1 and GR3 to GRn are normal, the signal from the check input terminal Rin

directly appears on the output line Rout at the timings T1 and T3 to Tn. However, since the output line GR2 is fixed at low level, the transistor 7b is turned off to change the output line Rout to low level at the timing T2.

As a result, at the timing T2, the output line GR2 is disconnected, and a scanning signal is supplied from the output line GL2 of the first scanning driver 4a so that a pulse appears on the second scanning line (L2,G2). In addition, at the timing Tn, the output line GLn is disconnected, and a scanning signal is supplied from the output line GRn of the second scanning driver 4b so that a pulse appears on the nth scanning line (Ln,Gn). In the above way, the defective points 10 to 12 are automatically corrected, and all lines are normally displayed.

The reason why the signal at the check input terminal Lin is not fixed at high level and is formed from pulses having a short low-level period at each timing will be described. For example, at the timing T1, the signal at the check input terminal Lin is changed to low level during the high-level period immediately before the selection period of the output line GL1 connected to the gate of the transistor 7a is ended. At this time, the transistor 7a is turned on, and the signal of the input terminal Lin is transmitted to the output line Lout to the judging

unit 5a to reset the output line Lout to low level. With this operation, unnecessary charges can be removed from the output line Lout of the judging unit 5a to cancel the previous state. If the signal of the input terminal Lin is fixed at high level, the output line Lout is not reset and becomes unstable. That is, unless the transistors 8a are temporarily turned off, the output lines GR1 to GRn affect on determination for the output lines GL1 to GLn, and which scanning driver 4a or 4b is being determined is unclear. To prevent this, the signals of the input terminals Lin and Rin must be pulsed.

(Second Embodiment)

Fig. 8 is a block diagram showing the structure of a liquid crystal display device according to the second embodiment of the present invention. The second embodiment is different from the first embodiment only in that n-channel MOS transistors 14a and 14b, p-channel MOS transistors 15a and 15b, and inverters 13a and 13b are provided in place of the switching transistors 8a and 8b in the first embodiment.

The portion on a first scanning driver 4a side will be described first. A CMOS (Complementary MOS) transistor made up from an n-channel MOS transistor 14a and a p-channel MOS transistor 15b forms a switch. One of the source and drain of each of the transistors 14a and 15a is connected to output lines

GL1 to GLn of the first scanning driver 4a, and the other is connected to scanning lines L1 to Ln in a display area 2. The gates of n-channel MOS transistors 14a are connected to the output of a judging unit 5a. A signal obtained by logically inverting the output from the judging unit 5a is input to the gates of p-channel MOS transistors 15a. The CMOS transistors (14a, 15a) function as switching units for connecting/disconnecting the output lines GL1 to GLn and scanning lines L1 to Ln.

In the portion on a second scanning driver 4b side as well, one of the source and drain of each of the n-channel MOS transistor 14b and the p-channel MOS transistor 15b is connected to output lines GR1 to GRn of the second scanning driver 4b, and the other is connected to scanning lines R1 to Rn in the display area 2. The gates of n-channel MOS transistors 14b are connected to the output of a judging unit 5b. A signal obtained by logically inverting the output from the judging unit 5b is input to the gates of p-channel MOS transistors 15b. The CMOS transistors (14b, 15b) function as switching units for connecting/disconnecting the output lines GR1 to GRn and scanning lines R1 to Rn.

In the second embodiment, by forming the switching units from the CMOS transistors (14a, 15a) and (14b, 15b), the switching speed can be increased as compared to the first embodiment that uses the

n-channel MOS transistors 8a and 8b. When the switching speed is increased, a scanning signal can be reliably supplied to the display area 2 at a predetermined timing, and the operation can be stabilized.

(Third Embodiment)

Fig. 9 is a block diagram showing the structure of a liquid crystal display device according to the third embodiment of the present invention. In the third embodiment, the output lines in first and second scanning drivers 71a and 71b are short-circuited to power supply line, so when a defect to fix an output line at high level is generated, the defect can be detected and automatically corrected.

In addition to a display area 2, a first data driver 3a, a second data driver 3b, a first scanning driver 71a, and a second scanning driver 71b, judging units 72a and 72b, NAND circuits 73a and 73b, inverters 74a, 74b, 76a, and 76b, n-channel MOS transistors 75a, 75b, 77a, and 77b, and p-channel MOS transistors 78a and 78b are integrally formed on a glass substrate 1.

The display area 2 and the first and second data drivers 3a and 3b are the same as in the first embodiment (Fig. 1). The first scanning driver 71a additionally has a 0th output line GL0 and (n+1)th output line GLn+1 as dummy lines, unlike the first

scanning driver 4a of the first embodiment (Fig. 1). The output lines GL0 and GLn+1 are not connected to the display area 2 but used to detect whether the output lines GL0 to GLn+1 of the first scanning driver 71a short-circuit to the power supply line. The second scanning driver 71b also additionally has a 0th output line GR0 and (n+1)th output line GRn+1 as dummy lines, unlike the second scanning driver 4b of the first embodiment (Fig. 1).

The inverters 76a and 76b, the n-channel MOS transistors 77a and 77b, and the p-channel MOS transistors 78a and 78b correspond to the inverters 13a and 13b, the n-channel MOS transistors 14a and 14b, and the p-channel MOS transistors 15a and 15b in the second embodiment (Fig. 8).

More specifically, the sources and drains of the MOS transistors 77a and 78a are connected to the output lines GL1 to GLn of the first scanning driver 71a and scanning lines L1 to Ln in the display area 2, respectively. The gates of the n-channel MOS transistors 77a are connected to the output of the judging unit 72a. The gates of the p-channel MOS transistors 78a are connected to the output of the judging unit 72a through the inverter 76a.

The sources and drains of the MOS transistors 77b and 78b are connected to the output lines GR1 to GRn of the second scanning driver 71b and scanning lines R1 to Rn in the display area 2, respectively. The

gates of the n-channel MOS transistors 77b are connected to the output of the judging unit 72b. The gates of the p-channel MOS transistors 78b are connected to the output of the judging unit 72b through the inverter 76b.

Each NAND circuit 73a has its input connected to two neighboring ones of the output lines GL0 to GLn+1 of the first scanning driver 71a and outputs the NAND result of scanning signals on the two output lines. Each inverter 74a receives the output from the corresponding NAND circuit 73a and outputs a logically inverted signal.

The check n-channel MOS transistors 75a correspond to the check transistors 7a in the first embodiment (Fig. 1). The gate of each check transistor 75a is connected to the output of the corresponding inverter 74a. One of the source and drain of each check transistor 75a is connected to a check input terminal Lin, and the other is connected to the input terminal of the judging unit 72a.

A check signal is input to the check input terminal Lin. When one of the output lines GL0 to GLn+1 is selected, the transistors 75a are turned on/off in accordance with the selection state. When a transistor 75a is turned on, the check signal input from the check input terminal Lin is output to the judging unit 72a.

The judging unit 72a determines in accordance

with the input of the check signal whether one or more output lines of the output lines GL0 to GLn+1 of the first scanning driver 71a are short-circuited to the power supply line and fixed at high level, and if so, outputs a low-level signal. Otherwise, the judging unit 72a outputs a high-level signal.

When the judging unit 72a outputs a high-level signal, the transistors 77a and 78a are turned on to connect the output lines GL1 to GLn of the first scanning driver 71a to the scanning lines L1 to Ln in the display area 2. Thus, the display area 2 can receive scanning signals from the first scanning driver 71a and be normally displayed.

On the other hand, when the judging unit 72a outputs a low-level signal, the transistors 77a and 78a corresponding to the abnormal output line are turned off to disconnect the abnormal output line of the output lines GL1 to GLn of the first scanning driver 71a from the corresponding one of the scanning lines L1 to Ln in the display area 2. This prevents the abnormal scanning signal from being supplied to the display area 2.

The first scanning driver 71a, the NAND circuits 73a, the inverters 74a and 76a, the transistors 75a, 77a, and 78a, and the first judging unit 72a have been described above. This also applies to the second scanning driver 71b, the NAND circuits 73b, the inverters 74b and 76b, the transistors 75b, 77b,

and 78b, and the second judging unit 72b.

Fig. 10 is a circuit diagram of the judging unit 72a shown in Fig. 9 and its peripheral portion. The judging unit 72a and its peripheral circuits will described below. This also applies to the judging unit 72b and its peripheral circuits. The scanning driver 71a additionally has a unit circuit AA for outputting the dummy output line GL0 and a unit circuit for outputting the dummy output line GLn+1, unlike the scanning driver 4a shown in Fig. 5A. The unit circuit AA has clocked inverters 81 and 83, an inverter 82, and an AND circuit 84, which correspond to the clocked inverters 54 and 56, the inverter 55, and the AND circuit 58 as an odd-numbered unit. For each of the clocked inverters 81, 53, and 54, referring to Fig. 4B, a clock bar signal terminal /CLK is connected to the gate of a transistor 41, and a clock signal terminal CLK is connected to the gate of a transistor 44. For each of the clocked inverters 83, 51, and 56, referring to Fig. 4B, the clock bar signal terminal /CLK is connected to the gate of the transistor 44, and the clock signal terminal CLK is connected to the gate of the transistor 41.

AND circuits 85a correspond to the combinations of the NAND circuits 73a and the inverters 74a in Fig. 9. The n-channel MOS transistors 75a and 77a, the p-channel MOS transistors 78a, and the inverter

76a correspond to the elements having the same reference numerals in Fig. 9.

The judging unit 72a has a D flip-flop 87, an inverter 88, a NAND circuit 89, a p-channel MOS transistor 90, and n-channel MOS transistors 86 and 92. The D flip-flop 87 has a clock terminal CK connected to the sources of the n-channel MOS transistors 75a through a signal line OH and an input terminal DF connected to an inverting output terminal /Q of its own. The n-channel MOS transistor 86 has its gate connected to a reset terminal RS, its drain connected to the input terminal DF, and its source connected to the ground terminal.

The inverter 88 has its input connected to the signal line OH and outputs the logically inverted signal of the input signal. The NAND circuit 89 has one input signal line A connected to the output of the inverter 88 and the other input signal line B connected to an output terminal Q of the D flip-flop 87. The p-channel MOS transistor 90 has its gate connected to a terminal SS, its source connected to the output of the NAND circuit 89, and its drain connected to the input of the inverter 76a. The n-channel MOS transistor 92 has its gate connected to the terminal SS, its drain connected to the input of the inverter 76a, and its source connected to the ground terminal.

Fig. 11 is a timing chart showing the operation

of the liquid crystal display device according to the third embodiment. This will be described by exemplifying a liquid crystal display device having no defect. Figs. 11 and 12 show the timing on the first scanning driver 71a side. The timing on the second scanning driver 71b side is the same as in Figs. 11 and 12.

Pulsed check signals are supplied to the check input terminals Lin and Rin, as in the first embodiment (Fig. 7). Normal pulsed scanning signals are sequentially output to the output lines GL0 to GLn+1 and GR0 to GRn+1.

The signal on a signal line H1 (Fig. 10) is the AND result of the signals on the output lines GL1 and GL2 and therefore holds low level. The signal on a signal line H2 (Fig. 10) is the AND result of the signals on the output lines GL2 and GL3 and therefore holds low level. When the signal lines H1, H2, and the like hold low level, all the n-channel MOS transistors 75a are turned off, so the signal line OH holds low level.

A pulsed reset signal is supplied to the reset terminal RS before the start timing of the scanning signal. The clock terminal CK of the D flip-flop 87 is connected to the signal line OH and holds low level, like the signal line OH. When the reset signal is input to the reset terminal RS, the input terminal DF of the D flip-flop 87 holds low level.

The input signal line A has a signal inverted from that on the signal line OH and holds high level. The input signal line B is connected to the output terminal Q of the D flip-flop 87 and holds low level. A signal line C has the NAND signal level of the signals on the signal lines A and B and therefore holds high level.

A pulse signal is supplied to the terminal SS. An input line E of the inverter 76a goes low when the terminal SS has a high-level signal, and has the same signal level as that on the signal line C when the terminal SS has a low-level signal. An output line F of the inverter 76a has a signal level inverted from that on the input line E.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level (i.e., when the signal line F is at low level), and goes low when the signal line E is at low level. Similarly, the scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level.

Consequently, the scanning signals on the output lines GL1 to GLn are sequentially normally supplied to the scanning lines L1 to Ln as pulses. Similarly, the scanning signals on the output lines GR1 to GRn are sequentially normally supplied to the scanning lines R1 to Rn as pulses.

Fig. 12 is a timing chart showing operation when the output line GL2 of the scanning driver 71a is short-circuited to the power supply line and fixed at high level in the liquid crystal display device according to the third embodiment.

Pulsed check signals are supplied to the check input terminals Lin and Rin. Only the output line GL2 is fixed at high level, and the remaining output lines GL0, GL1, and GL3 to GLn+1 sequentially output normal pulsed scanning signals.

Since the signal on the signal line H1 is the AND result of the signals on the output lines GL1 and GL2, a pulse is output at a timing T1. Since the signal on the signal line H2 is the AND result of the signals on the output lines GL2 and GL3, a pulse is output at a timing T3.

The signal line OH has the same signal level as that of the signal of the check input terminal Lin when the signal on the signal line H1 or H2 goes high, and otherwise, goes low. As a result, the signal line OH outputs a pulse only at the timings T1 and T3, and holds low level during the remaining period. The signals at the terminals RS and SS are the same as in Fig. 11.

The clock terminal CK of the D flip-flop 87 has the same signal level as that on the signal line OH. The input terminal DF of the D flip-flop 87 changes from low level to high level at the timing T3 in

accordance with the second leading edge of the signal at the clock terminal CK.

A signal inverted from that on the signal line OH is supplied to the input signal line A. The signal level on the input signal line B is inverted in accordance with the leading edge at the clock terminal CK of the D flip-flop 87. That is, the signal level changes from low level to high level at the timing T1 and from high level to low level at the timing T3. The signal line C has the NAND signal level of the signals on the signal lines A and B.

The input line E of the inverter 76a goes low when the signal at the terminal SS is at high level, and has the same signal level as that on the signal line C when the signal at the terminal SS is at low level. The output line F of the inverter 76a has a signal level inverted from that on the input line E.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is at low level. Similarly, the scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level.

As a result, the scanning line L1 outputs a pulse at the timing T1, as in Fig. 12. However, for the scanning line L2, since the output line GL2 is short-circuited to the power supply line, no pulse is

output at a timing T2 when a pulse should be output. Instead, at the timing T2, a normal scanning signal is supplied from the output line GR2 of the second scanning driver 71b to the scanning line R2 in the display area 2, so normal display is performed.

(Fourth Embodiment)

A liquid crystal display device according to the fourth embodiment of the present invention is different from the third embodiment (Fig. 9) only in the structure of judging units 72a and 72b. According to the fourth embodiment, when a defect is generated, with which two or more neighboring (continuous) output lines of a first or second scanning driver 71a or 71b are short-circuited to the power supply line and fixed at high level, the defect can be detected and automatically corrected. When two or more neighboring output lines of the first scanning driver 71a short-circuit to the power supply line, all output lines of the first scanning driver 71a are disconnected from a display area 2, and scanning signals are supplied from the output lines of the second scanning driver 71b to the display area 2. On the other hand, when two or more neighboring output lines of the second scanning driver 71b short-circuit to the power supply line, all output lines of the second scanning driver 71b are disconnected from the display area 2, and scanning signals are supplied from the output lines of the

first scanning driver 71a to the display area 2.

Fig. 13 is a circuit diagram of the judging unit 72a according to the fourth embodiment and its peripheral portion. The judging unit 72a and its peripheral circuits will be described below. This also applies to the judging unit 72b and its peripheral portion. The judging unit 72a additionally has a base-n counter 133, an n-channel MOS transistor 132, a latch circuit 134, an inverter 135, and an AND circuit 136.

The base-n counter 133 has its input terminal NCK connected to a signal line OH and its reset terminal NR connected to the drain of the n-channel MOS transistor 132. The base-n counter 133 counts N pulses and then outputs a high-level signal from an output terminal NQ. The n-channel MOS transistor 132 has its source connected to the ground terminal and its gate connected to a reset terminal RS.

For example, when the horizontal resolution in the display area of the liquid crystal display device is 600; N = 600. The base-n counter 133 counts N pulses in one frame and then outputs a high-level signal from the output terminal NQ. When the number of pulses in one frame is smaller than N, the base-n counter 133 resets the count value at every frame and outputs a low-level signal from the output terminal NQ.

The latch circuit 134 has its set terminal S

connected to the output terminal NQ of the base-n counter 133 and its reset terminal R connected to the ground terminal. When a high-level signal is input to the set terminal S, the latch circuit 134 outputs a high-level signal from an output terminal Q0. The inverter 135 has its input terminal connected to the output terminal Q0 of the latch circuit 134 and outputs an output signal inverted from the input signal to a signal line N.

The output terminal of a NAND circuit 89 is connected to a signal line C, like the NAND circuit 89 (Fig. 10) in the judging unit 72a of the third embodiment. The AND circuit 136 having its input terminals connected to the signal lines C and N performs an AND operation between the signals of these signal lines and outputs an output signal to a signal line G. A p-channel MOS transistor 90 has its source connected to the signal line G, its drain connected to a signal line E, and its gate connected to a terminal SS. An n-channel MOS transistor 92 has its source connected to the ground terminal, its drain connected to the signal line E, and its gate connected to the terminal SS. An inverter 76a has its input terminal connected to the signal line E and outputs an output signal inverted from the input signal to a signal line F. The signal line E is connected to the gates of n-channel MOS transistors 77a. The signal line F is connected to the gates of

p-channel MOS transistors 78a.

Fig. 14 is a timing chart showing the operation of the liquid crystal display device according to the fourth embodiment. This will be described by exemplifying a liquid crystal display device having no defect. Figs. 14 to 16 show the timing on the first scanning driver 71a side. The timing on the second scanning driver 71b side is the same as in Figs. 14 to 16.

A pulsed check signal is supplied to a check input terminal Lin, as in the third embodiment (Fig. 11). Output lines GL0 to GLn+1 sequentially output normal pulsed scanning signals.

A signal line H1 has the AND signal level of the signals on the output lines GL1 and GL2 and therefore holds low level. A signal line H2 has the AND signal level of the signals on the output lines GL2 and GL3 and therefore holds low level. All transistors 75a are then turned off, and the signal line OH also holds low level.

The same signals as in the third embodiment (Fig. 11) are input to the reset terminal RS and terminal SS. A clock terminal CK of a D flip-flop 87 has the same signal level as on the signal line OH and holds low level. When a reset signal is input to the reset terminal RS, an input terminal DF of the D flip-flop 87 holds low level.

An input line A has a signal inverted from that

on the signal line OH and holds high level. An input line B is connected to an output terminal Q of the D flip-flop 87 and holds low level. The signal line C has the NAND signal level of the signals on the signal lines A and B and therefore holds high level.

Since the signal line OH connected to the input terminal NCK of the base-n counter 133 holds low level, the output terminal NQ also holds low level. Since the output terminal NQ connected to the set terminal S of the latch circuit 134 holds low level, the output terminal Q0 of the latch circuit 134 also holds low level. The signal line N has a signal level inverted from that on the output terminal Q0 and therefore holds high level.

The signal line G has the AND signal level of the signals on the signal lines N and C and holds high level. The input line E of the inverter 76a goes low when the terminal SS has a high-level signal, and has the same signal level as that on the signal line G when the terminal SS has a low-level signal. The output line F of the inverter 76a has a signal level inverted from that on the input line E.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is at low level. Hence, a pulse is output at a timing T1. Similarly, the scanning line L2 has the same signal level as that on the output line GL2 when the

signal line E is at high level, and goes low when the signal line E is at low level. Hence, a pulse is output at a timing T2.

Consequently, the scanning signals on the output lines GL1 to GLn are normally supplied to the scanning lines L1 to Ln. Similarly, the scanning signals on the output lines GR1 to GRn are normally supplied to the scanning lines R1 to Rn.

Fig. 15 is a timing chart showing operation when the output line GL2 of the scanning driver 71a is short-circuited to the power supply line and fixed at high level in the liquid crystal display device according to the fourth embodiment.

A pulsed check signal is supplied to the check input terminal Lin. Only the output line GL2 is fixed at high level, and the remaining output lines GL0, GL1, and GL3 to GLn+1 sequentially output normal pulsed scanning signals.

Since the signal line H1 has the AND signal level of the signals on the output lines GL1 and GL2, a pulse is output at the timing T1. Since the signal line H2 has the AND signal level of the signals on the output lines GL2 and GL3, a pulse is output at a timing T3.

The signal line OH has the same signal level as that of the signal of the check input terminal Lin when the signal on the signal line H1 or H2 goes high, and otherwise, goes low. As a result, the signal

line OH outputs a pulse only at the timings T1 and T3, and holds low level during the remaining period. The signals at the terminals RS and SS are the same as in Fig. 14.

The clock terminal CK of the D flip-flop 87 has the same signal level as that on the signal line OH. The input terminal DF of the D flip-flop 87 changes from low level to high level at the timing T3 in accordance with the second leading edge of the signal at the clock terminal CK.

The input line A has a signal level inverted from that on the signal line OH. The signal level on the input line B is inverted in accordance with the leading edge of the signal at the clock terminal CK of the D flip-flop 87. That is, the signal level changes from low level to high level at the timing T1 and from high level to low level at the timing T3. The signal line C has the NAND signal level of the signals on the signal lines A and B.

The signal line OH connected to the input terminal NCK of the base-n counter (e.g., N = 600) 133 includes only two pulses per frame, so the base-n counter 133 resets the value every frame, and its output terminal NQ holds low level. Since the output terminal NQ connected to the set terminal S of the latch circuit 134 holds low level, the output terminal Q0 of the latch circuit 134 also holds low level. The signal line N has a signal level inverted

from that at the output terminal Q0 and therefore holds high level.

The signal line G has the AND signal level of the signals on the signal lines N and C and therefore has the same signal level as that on the signal line C. The input line E of the inverter 76a goes low when the signal at the terminal SS is at high level, and has the same signal level as that on the signal line G when the signal at the terminal SS is at low level. The output line F of the inverter 76a has a signal level inverted from that on the input line E.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is at low level. Similarly, the scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level.

As a result, the scanning line L1 outputs a pulse at the timing T1, as in Fig. 14. However, for the scanning line L2, since the output line GL2 is short-circuited to the power supply line and disconnected, no pulse is output at the timing T2 when a pulse should be output. Instead, at the timing T2, a normal scanning signal is supplied from the output line GR2 of the second scanning driver 71b to the scanning line R2 in the display area 2, so normal display is performed.

Fig. 16 is a timing chart showing operation when the neighboring (consecutive) output lines GL2 and GL3 of the scanning driver 71a are short-circuits to the power supply line and fixed at high level in the liquid crystal display device according to the fourth embodiment.

A pulsed check signal is supplied to the check input terminal Lin. Only the output lines GL2 and GL3 are fixed at high level, and the remaining output lines GL0, GL1, and GL4 to GLn+1 sequentially output normal pulsed scanning signals.

Since the signal line H1 has the AND signal level of the signals on the output lines GL1 and GL2, a pulse is output at the timing T1. The signal line H2 has the AND signal level of the signals on the output lines GL2 and GL3 and therefore holds high level.

Since the signal line H2 holds high level, the transistor 75a connected to the signal line H2 holds the ON state, and the signal line OH has the same signal level as that of the signal at the check input terminal Lin. The signals at the terminals RS and SS are the same as those shown in Fig. 14.

The clock terminal CK of the D flip-flop 87 has the same signal level as that on the signal line OH. The input terminal DF of the D flip-flop 87 inverts the signal level in accordance with the second and subsequent leading edges of the signal at the clock terminal CK.

A signal inverted from that on the signal line OH is supplied to the input line A. The signal level on the input signal line B is inverted in accordance with the leading edge of the signal at the clock terminal CK. The signal line C has the NAND signal level of the signals on the signal lines A and B.

When the horizontal resolution of the display area 2 is 600 (n = 600), the signal line OH connected to the input terminal NCK of the base-n counter (N = 600) 133 includes 600 pulses per frame. Hence, the base-n counter 133 counts the 600th pulse on the signal line OH at a timing Tn, so the output terminal NQ changes from low level to high level.

Since the output terminal NQ is connected to the set terminal S of the latch circuit 134, the output terminal Q0 of the latch circuit 134 outputs a signal 141 in the first frame and a signal 142 in the second and subsequent frames. The signal 141 of the first frame changes from low level to high level at the timing Tn in accordance with the leading edge of the signal at the output terminal NQ of the base-n counter 133. The signal 142 of the second and subsequent frames continuously holds high level. From the second frame, the signal line N has a signal level inverted from that at the output terminal Q0 and therefore holds low level.

The signal line G has the AND signal level of the signals on the signal lines N and C and thus goes low.

The input line E of the inverter 76a goes low when the terminal SS has a high-level signal, and has the same signal level as that on the signal line G when the terminal SS has a low-level signal. As a result, the signal line E holds low level. The output line F of the inverter 76a has a signal level inverted from that on the input line E and therefore holds high level.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is at low level. Hence, the scanning line L1 outputs no pulse at the timing T1 when a pulse should be output, and holds low level. The scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level. Hence, the scanning line L2 outputs no pulse at the timing T2 when a pulse should be output, and holds low level.

That is, all the output lines GL1 to GLn of the first scanning driver 71a are disconnected from the display area 2, and no pulses are supplied from the first scanning driver 71a to the scanning lines L1 to Ln. Instead, normal scanning signals are supplied from the second scanning driver 71b to all the scanning lines R1 to Rn in the display area 2, and normal display is performed.

According to the fourth embodiment, when two or

more neighboring output lines, e.g., the output lines GL2 and GL3, among the output lines GL0 to GLn+1 are fixed at high level, all the output lines GL1 to GLn of the first scanning driver 71a are disconnected from all the scanning lines L1 to Ln in the display area 2 by the switching transistors. Instead, the second scanning driver 71b supplies scanning signals to all the scanning lines R1 to Rn in the display area 2 through the output lines GR1 to GRn, respectively. Hence, the liquid crystal display device can perform normal display on all the lines.

(Fifth Embodiment)

Fig. 17 is a block diagram showing the structure of a liquid crystal display device according to the fifth embodiment of the present invention. In the fifth embodiment, the second embodiment (Fig. 8) and the third embodiment (Fig. 9) are integrated. In the fifth embodiment, when a defect is generated, with which an output line in first or second scanning driver 71a or 71b short-circuits to the ground line or power supply line or is unfixed and is fixed at low or high level, the defect can be detected and automatically corrected.

A glass substrate 1, a display area 2, data drivers 3a and 3b, scanning drivers 71a and 71b, NAND circuits 73a and 73b, inverters 74a, 74b, 76a, and 76b, and MOS transistors 75a, 75b, 77a, 77b, 78a, and 78b are the same as those shown in the third

embodiment (Fig. 9). Check n-channel MOS transistors 93a and 93b correspond to the check n-channel MOS transistors 7a and 7b in the second embodiment (Fig. 8).

A judging unit 94a receives signals from the sources of the n-channel MOS transistors 75a and the sources of the n-channel MOS transistors 93a and outputs signals to the gates of the n-channel MOS transistors 77a and the input terminal of the inverter 76a. A judging unit 94b has the same structure as that of the judging unit 94a.

Fig. 18 is a circuit diagram of the judging unit 94a shown in Fig. 17 and its peripheral portion. The judging unit 94a and its peripheral circuits will be described below. This also applies to the judging unit 94b and its peripheral circuits. The scanning driver 71a is the same as that shown in the third embodiment (Fig. 10).

AND circuits 85a correspond to the combinations of the NAND circuits 73a and the inverters 74a in Fig. 17. The same reference numerals as in Fig. 17 denote the same elements as in Fig. 17.

The judging unit 94a additionally has an AND circuit 95, unlike the judging unit 72a shown in the third embodiment (Fig. 10). The AND circuit 95 has one input line C connected to the output of a NAND circuit 89 and the other input line D connected to the sources of the n-channel MOS transistors 93a

through a signal line OL. The output of the AND circuit 95 is connected to the source of a p-channel MOS transistor 90. An n-channel MOS transistor 92 is connected in the same way as in the third embodiment (Fig. 10).

Fig. 19 is a timing chart showing the operation of the liquid crystal display device according to the fifth embodiment when the liquid crystal display device has no defect. Figs. 19 to 21 show the timing on the first scanning driver 71a side. The timing on the second scanning driver 71b side is the same as in Figs. 19 to 21.

Pulsed check signals are supplied to check input terminals Lin and Rin, as in the first embodiment (Fig. 7). Output lines GL0 to GLn+1 and GR0 to GRn+1 sequentially output normal pulsed scanning signals.

A signal line H1 has the AND signal level of the signals on the output lines GL1 and GL2 and therefore holds low level. A signal line H2 has the AND signal level of the signals on the output lines GL2 and GL3 and therefore holds low level. Since the signal lines H1, H2, and the like hold low level, all the transistors 75a are turned off, so the signal line OH holds low level.

Since the transistors 93a are turned on in accordance with the pulses on the output lines GL1, GL2, GL3, and the like, the same signal as the signal at the check input terminal Lin appears on the signal

line OL connected to the sources of the transistors 93a. The same signals as in the third embodiment (Fig. 11) are supplied to terminals RS and SS.

A clock terminal CK of a D flip-flop 87 has the same signal level as that on the signal line OH and holds low level. When a reset signal is input to the reset terminal RS, an input terminal DF of the D flip-flop 87 holds low level.

An input line A has a signal inverted from that on the signal line OH and holds high level. An input line B is connected to an output terminal Q of the D flip-flop 87 and holds low level.

The signal line C has the NAND signal level of the signals on the signal lines A and B and therefore holds high level. The signal line D has the same signal level as that on the signal line OL. A signal line G has the AND signal level of the signals on the signal lines C and D and therefore has the same signal level as on the signal line D. An input line E of the inverter 76a goes low when the terminal SS has a high-level signal, and has the same signal level as that on the signal line G when the terminal SS has a low-level signal. An output line F of the inverter 76a has a signal level inverted from that on the input line E.

A scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is

at low level. Hence, a pulse is output at a timing T1. Similarly, a scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level. Hence, a pulse is output at a timing T2.

Consequently, the scanning signals on the output lines GL1 to GLn are normally supplied to the scanning lines L1 to Ln. Similarly, the scanning signals on the output lines GR1 to GRn are normally supplied to the scanning lines R1 to Rn.

Fig. 20 is a timing chart showing operation when the output line GL2 of the scanning driver 71a is short-circuited to the ground line and fixed at low level or is disconnected and unfixed in the liquid crystal display device according to the fifth embodiment.

A pulsed check signal is supplied to the check input terminal Lin. Only the output line GL2 is fixed at low level, and the remaining output lines GL0, GL1, and GL3 to GLn+1 sequentially output normal pulsed scanning signals.

The signal line H1 has the AND signal level of the signals on the output lines GL1 and GL2 and therefore holds low level. The signal line H2 has the AND signal level of the signals on the output lines GL2 and GL3 and therefore holds low level. Since the signal lines H1, H2, and the like hold low

level, all the transistors 75a are turned off, so the signal line OH holds low level.

The signal line OL has the same signal level as that at the check input terminal Lin when the output lines GL1, GL2, GL3, and the like are at high level. As a result, the signal line OL holds low level at the timing T2 and outputs a pulse at the remaining timings T1 and T3 to Tn. The signals at the terminals RS and SS are the same as in Fig. 19.

The clock terminal CK of the D flip-flop 87 has the same signal level as that on the signal line OH and holds low level. The input terminal DF of the D flip-flop 87 holds low level in accordance with the reset signal at the reset terminal RS.

The input line A has a signal inverted from that on the signal line OH and holds high level. The input line B is connected to the output terminal Q of the D flip-flop 87 and holds low level. One input line C of the AND circuit 95 has the NAND signal level of the signals on the signal lines A and B and holds high level. The other signal line D has the same signal level as that on the signal line OL. The signal line G has the AND signal level of the signals on the input lines C and D and therefore has the same signal level as on the input line D.

The input line E of the inverter 76a goes low when the terminal SS has a high-level signal, and has the same signal level as that on the signal line G

when the terminal SS has a low-level signal. The output line F of the inverter 76a has a signal level inverted from that on the input line E.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is at low level. Hence, a pulse is output at the timing T1. The scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level. However, no pulse is output at the timing T2 when a pulse should be output.

Consequently, the normal scanning signals on the output lines GL1 and GL3 to GLn are supplied to the scanning lines L1 and L3 to Ln. For the scanning line L2, however, since the output line GL2 is short-circuited to the ground line, no pulse is output a the timing T2 when a pulse should be output. Instead, at the timing T2, a normal scanning signal is supplied from the second scanning driver 71b to the scanning line R2 in the display area 2, and normal display is performed.

Fig. 21 is a timing chart showing operation when the output line GL2 of the scanning driver 71a is short-circuited to the power supply line and fixed at high level in the liquid crystal display device according to the fifth embodiment.

A pulsed check signal is supplied to the check

input terminal Lin. Only the output line GL2 is fixed at high level, and the remaining output lines GL0, GL1, and GL3 to GLn+1 sequentially output normal pulsed scanning signals.

Since the signal line H1 has the AND signal level of the signals on the output lines GL1 and GL2, a pulse is output at the timing T1. Since the signal line H2 has the AND signal level of the signals on the output lines GL2 and GL3, a pulse is output at the timing T3. The signal line OH has the same signal level as that of the signal of the check input terminal Lin when the signal on the signal line H1 or H2 goes high. As a consequence, the signal line OH outputs a pulse at the timings T1 and T3. Since the output line GL2 is fixed at high level, the transistors 93a hold the ON state, and the same signal as that at the check input terminal Lin is output to the signal line OL. The signals at the terminals RS and SS are the same as those shown in Fig. 19.

The clock terminal CK of the D flip-flop 87 has the same signal level as that on the signal line OH. The input terminal DF of the D flip-flop 87 changes from low level to high level at the timing T3 in accordance with the second leading edge of the signal at the clock terminal CK.

A signal inverted from the signal on the signal line OH is supplied to the input line A. The signal

level on the input line B is inverted in accordance with the leading edge of the signal at the clock terminal CK of the D flip-flop 87. Hence, the signal level changes from low level to high level at the timing T1 and from high level to low level at the timing T3.

One input line C of the AND circuit 95 has the NAND signal level of the signals on the signal lines A and B and holds low level during the period of timing T2. The other input line D has the same signal level as that of the signal on the signal line OL. The signal line G has the AND signal level of the signals on the input lines C and D.

The input line E of the inverter 76a goes low when the signal at the terminal SS is at high level, and has the same signal level as that on the signal line G when the signal at the terminal SS is at low level. The output line F of the inverter 76a has a signal level inverted from that on the input line E.

The scanning line L1 has the same signal level as that on the output line GL1 when the signal line E is at high level, and goes low when the signal line E is at low level. Similarly, the scanning line L2 has the same signal level as that on the output line GL2 when the signal line E is at high level, and goes low when the signal line E is at low level. As a result, the scanning line L1 outputs a pulse at the timing T1. However, for the scanning line L2, since the output

line GL2 is short-circuited to the power supply line, no pulse is output at the timing T2 when a pulse should be output. Instead, at the timing T2, a normal scanning signal is supplied from the output line GR2 of the second scanning driver 71b to the scanning line R2 in the display area 2, so normal display is performed.

According to the fifth embodiment, even when a defect is generated to short-circuit an output line of the first or second scanning driver 71a or 71b to the ground line and fix the output line at low level, or a defect is generated to short-circuit an output line to the power supply line and fix the output line at high level, these defects can be detected and automatically corrected. Hence, the liquid crystal display device can perform normal display on all lines.

The judging unit 72a (Fig. 13) of the liquid crystal display device according to the fourth embodiment may be applied to the liquid crystal display device (Fig. 17) according to the fifth embodiment. In this case, for example, when two or more neighboring output lines of the first scanning driver 71a are fixed at high or low level, all the output lines GL1 to GLn of the first scanning driver 71a are disconnected from all the scanning lines L1 to Ln in the display area 2 by switching transistors, so scanning signals can be supplied from the second

scanning driver 71b to all the scanning lines R1 to Rn in the display area 2.

As has been described above, according to the first and second embodiments, when an output line of the scanning driver is short-circuited to the ground line and fixed at low level, or disconnected and unfixed, the fixed or unfixed output line can be detected and automatically corrected. According to the third and fourth embodiments, when an output line of the scanning driver is short-circuited to the power supply line and fixed at high level, the fixed or unfixed output line can be detected and automatically corrected. According to the fifth embodiment, when an output line of the scanning driver is short-circuited to the ground line or power supply line and fixed at low or high level, or disconnected and unfixed, the fixed or unfixed output line can be detected and automatically corrected.

According to the fourth embodiment, when the judging unit determines that the potentials of two or more neighboring output lines of the first scanning driver are fixed, the switching transistors can disconnect all the output lines of the first scanning driver from all the scanning lines in the display area, and all the scanning signals can be supplied from the second scanning driver to the display area. In addition, when it is determined that the potentials of two or more neighboring output lines of

the second scanning driver are fixed, all the output lines of the second scanning driver can be disconnected from all the scanning lines in the display area, and all the scanning signals can be supplied from the first scanning driver to the display area. Thus, the liquid crystal display device can perform normal display.

According to the first to fifth embodiments, when the potential of an output line of the first or second scanning driver is fixed, only the fixed output line can be disconnected from the corresponding scanning line in the display area. For example, when an output line of the first scanning driver is disconnected from the corresponding scanning line in the display area, a normal scanning signal is supplied from the corresponding output line of the second scanning driver to the scanning line in the display area. Instead of disconnecting all the output lines of the first or second scanning driver from all the scanning lines in the display area, only the output line with the fixed potential can be disconnected from the scanning line in the display area. For this reason, the normal output lines of the first or second scanning driver and the scanning lines in the display area are connected, so normal display can be performed. In addition, since it is determined individually for the first and second scanning drivers whether the potential of an output

line is fixed, and the output lines are individually disconnected from the scanning lines as needed, even defects as shown in Figs. 25 and 26 can be corrected. That is, even when defects are present at portions, e.g., both of the first or second scanning driver and the display area have defects, or the first and second scanning drivers and display area have defects, the defects can be reliably detected and automatically corrected, so normal display can be performed.

Since the automatic correction is possible, the yield of liquid crystal display devices can be increased, the productivity can be improved, and the cost of liquid crystal display devices can be reduced.

A case in which the defective/non-defective state of a scanning signal in the first and second scanning drivers is determined, and the output line and scanning line are disconnected in accordance with the determination result has been described. The same implementation may be applied to the first and second data drivers. More specifically, the first and second data drivers may supply identical data signals to the display area, the defective/non-defective state of a data signal in the first and second data drivers may be determined, and the data line between the data driver and the display area may be disconnected in accordance with the determination result.

The above embodiments are merely examples of the present invention and should not be construed to limit the technical range of the present invention. That is, the present invention can be practiced in various forms without departing from its technical spirit and scope or major features.